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ATTORNEY'S DOCKET NO.: S1022.80201US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Pierrick DESCURE	
Serial No.:	09/361,700	Patent No. 6,960,799 B2
Filed:	July 27, 1999	Issued: November 1, 2005
For:	IMAGE SENSOR WITH A PHOTODIODE ARRAY	

Examiner: Gene M. Munson
Art Unit: 2811 Confirmation No.: 5850

ATTN: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

Transmitted herewith for filing is/are the following document(s):

[X] Request for Certificate of Correction
[X] Copies of: Pages 1-4 of 02/11/05 Amn. and Cols. 4-5 of U.S. Patent No. 6,960,799.
[X] PTO Form SB/44
[X] Return Post Card

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned collect at (617) 646.8000, Boston, Massachusetts.

No check is enclosed. If it is determined that a fee is necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Correspondence and Mail Division, Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the 9th day of November, 2005.

Attorney Docket No.: S1022.80772US00
XNDD

Respectfully submitted,

Pierrick Descure, Applicant

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REQUEST FOR CERTIFICATE
OF CORRECTION UNDER 37 C.F.R. §1.323

Sir/Madam:

Patentees respectfully request the correction of errors found in the above-captioned patent. Specifically, there are typographical errors in claims 10 and 12 of issued U.S. Patent No. 6,960,799 B2.

Claim 10, as it appears in column 4, line 66 through column 5, line 3, of U.S. Patent No. 6,960,799 is reproduced below.

> 10. The array of photodiodes of claim 9, wherein said single-crystal silicon layer and said polysilicon layer have a high refraction coefficient on the order of 4, while said silicon oxide layer and silicon nitride layer have a lower **refract on** coefficient, on the order of 1.5. (Emphasis added)

Claim 10, as it appeared in the Amendment After Final filed on February 11, 2005 is reproduced below.

> 10. The array of photodiodes of claim 9, wherein said single-crystal silicon layer and said polysilicon layer have a high refraction coefficient on the order of 4, while said silicon oxide layer and silicon nitride layer have a lower **refraction** coefficient, on the order of 1.5. (Emphasis added)

No amendment was made by the Examiner or Patentee to change "refraction" to "refract on" in the last line of this claim.

Claim 12, found in column 5, lines 8-16, of U.S. Patent No. 6,960,799 is reproduced below.

> 12. The array of photodiodes of claim 1, wherein the at least one insulating layer includes a first insulating layer and a second insulating layer disposed below the first insulating layer, the first insulating layer extending across three photodiodes each in a different one of the three interleaved sub-arrays, and the second insulating layer extending across at least two photodiodes of the three photodiodes, wherein said **at least on** conductive layer extends across each of the three photodiodes above the first insulating layer. (Emphasis added)

Claim 12 of U.S. Patent No. 6,960,799, as it appeared in the Amendment After Final (as claim 28) filed on February 11, 2005 is reproduced below.

> 28. The array of photodiodes of claim 1, wherein the at least one insulating layer includes a first insulating layer and a second insulating layer disposed below the first insulating layer, the first insulating layer extending across three photodiodes each in a different one of the three interleaved sub-arrays, and the second insulating layer extending across at least two photodiodes of the three photodiodes, wherein said **at least one** conductive layer extends across each of the three photodiodes above the first insulating layer. (Emphasis added)

No amendment was made by the Examiner or Patentee to change "at least one" to "at least on" in line 15 of this claim. Patentee desires to have the claim read --refraction-- as filed and respectfully request that a Certificate of Correction be granted in U.S. Letters Patent No. 6,960,799 to make the corrections as specified herein and on the attached Certificate of Correction, PTO form SB/44.

No amendment was made by the Examiner or Patentees to change "according to" to "of" in line 1 of this claim.

In support of the above, Patentees enclose a highlighted copy of pages 1-4 of the Amendment After Allowance filed on February 11, 2005 and columns 4-5 of issued U.S. Patent No. 6,960,799. Also enclosed is a Certificate of Correction form PTO Form SB/44.

The corrections requested do not involve change in the patent that constitutes new matter or would require reexamination. Therefore, it is respectfully requested that the correction be made and that a Certificate of Correction be issued.

Since neither of the above amendments were made by either Patentee or the Examiner it is respectfully requested that the corrections as specified herein and on the attached Certificate of Correction, PTO form SB/44 be made and a Certificate of Correction be granted. Patentee respectfully submits that, since the errors for which a Certificate of Correction is sought was the result of Patent Office mistake, no fee is due. However, if the Examiner deems a fee necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825.

Should any questions arise concerning the foregoing, please contact the undersigned at the telephone number listed below.

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Gail Driscoll

Attorney Docket No.: S1022.80772US00
XNDD

Respectfully submitted,

Pierrick Descure, Applicant

By:

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PTO/SB/44 (04-04)
Approved for use through 04/30/2007
U.S. Patent and Trademark Office; US. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.	:	6,960,799 B2
DATED	:	November 1, 2005
INVENTOR(S)	:	Pierrick Descure

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 10, col. 5, line 3 should read:
--refraction coefficient, on the order of 1.5.--

Claim 12, col. 5, line 15 should read:
--said at least one conductive layer extends across each of the--

MAILING ADDRESS OF SENDER

PATENT NO. 6,960,799

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NOV 21 2005

RESPONSE UNDER 37 C.F.R. §1.116
- EXPEDITED PROCEDURE-
EXAMINING GROUP 2811

DOCKET NO: S1022.80201US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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The undersigned hereby certifies that this document and the listed enclosures are being placed in the United States mail with first-class postage attached, addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February 11, 2005.

Eileen MacKenzie

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AFTER FINAL

Sir:

In response to the Office Action mailed October 14, 2004, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims that begins on page 2 of this amendment.

Remarks begin on page 6 of this amendment.

IN THE CLAIMS

Please cancel claims 12-18, 32-34, and 36-39 without prejudice or disclaimer.

Please replace all prior versions, and listings, of claims in the application with the following list of claims:

1. (Previously Presented) An array of photodiodes made of regions of a second conductivity type formed in a semiconductive region of a first conductivity type, divided into three interleaved sub-arrays, each sub-array corresponding to a respective color of light, all photodiodes of a respective sub-array being coated with a same interference filter including at least one insulating layer of determined thickness coated with at least one conductive layer, a combined thickness of the at least one insulating layer and the at least one conductive layer being different for each sub-array, the determined thickness of said at least one insulating layer and said at least one conductive layer coating the respective sub-array determining the respective color of light that is interferentially filtered and provided to the respective sub-array, wherein the determined thickness of said at least one insulating layer is proportional to a wavelength of the color of light that is interferentially filtered, wherein said at least one conductive layer is electrically connected to the semiconductive region of the first conductivity type.

2. (Original) The array of photodiodes of claim 1, wherein the electric connection is indirect.

3. (Original) The array of photodiodes of claim 1, wherein the semiconductor substrate is a single-crystal silicon substrate, and the interference filter includes a silicon oxide layer formed above the substrate and a conductive polysilicon layer formed above the silicon oxide layer.

4. (Previously Presented) The array of photodiodes of claim 1, wherein the semiconductive region of the first conductivity type comprises a semiconductor substrate made of single-crystal silicon.

5. (Original) The array of photodiodes of claim 1, wherein said at least one insulating layer comprises a silicon oxide layer.

6. (Previously Presented) The array of photodiodes of claim 1, wherein said at least one conductive layer comprises a polysilicon layer.

7. (Previously Presented) The array of photodiodes of claim 1, further comprising a silicon nitride layer over said at least one conductive layer.

8. (Previously Presented) The array of photodiodes of claim 1, wherein said semiconductive region of the first conductivity type comprises a semiconductor substrate made of single-crystal silicon, said at least one insulating layer comprises a silicon oxide layer, and said at least one conductive layer comprises a polysilicon layer.

9. (Previously Presented) The array of photodiodes of claim 8, further comprising a silicon nitride layer over said at least one conductive layer.

10. (Previously Presented) The array of photodiodes of claim 9, wherein said single-crystal silicon layer and said polysilicon layer have a high refraction coefficient on the order of 4, while said silicon oxide layer and silicon nitride layer have a lower refraction coefficient, on the order of 1.5.

11. (Previously Presented) The array of photodiodes of claim 1, wherein said at least one conductive layer is connected to said semiconductive region of the first conductivity type at a heavily doped P-type region thereof.

12-18. (Canceled)

19-26. (Canceled)

27. (Previously Presented) A photodiode comprising:

a semiconductor substrate of a first conductivity type;

a semiconductive region of a second conductivity type formed in said semiconductor substrate;

a multilayer interference filter disposed over said semiconductive region and including;

at least one insulating layer having a predetermined thickness, and

a conductive layer disposed over said at least one insulating layer,

said semiconductor substrate defining a well formed in a base substrate of the second conductivity type, said conductive layer being electrically connected to said base substrate,

wherein the predetermined thickness of said at least one insulating layer, in combination with said conductive layer, is adapted to interferentially filter a particular wavelength of light; and

wherein the predetermined thickness of said at least one insulating layer is proportional to the particular wavelength of light.

28. (Previously Presented) The array of photodiodes of claim 1, wherein the at least one insulating layer includes a first insulating layer and a second insulating layer disposed below the first insulating layer, the first insulating layer extending across three photodiodes each in a different one of the three interleaved sub-arrays, and the second insulating layer extending across at least two photodiodes of the three photodiodes, wherein said at least one conductive layer extends across each of the three photodiodes above the first insulating layer.

groups of cathode regions 1R, 1G, 1B respectively sensitive to red, to green, and to blue.

In a first step illustrated in FIG. 2A, a first silicon oxide layer 4-1 is deposited and etched to maintain it in place only above regions 1R.

In a second step illustrated in FIG. 2B, a second silicon oxide layer 4-2 is deposited and etched to only leave it in place above regions 1R and 1G.

In a third step illustrated in FIG. 2C, a third silicon oxide layer 4-3 is deposited and left in place. After this, a polysilicon layer 5 and possibly, as previously described, a silicon nitride layer, are deposited. Then, the structure is properly etched to enable making contacts at selected locations.

The thickness of layer 4-3, in the case of the example given previously, is 150 nm, and the thicknesses of layers 4-1 and 4-2 are 40 nm so that oxide layers having respective thicknesses of 230, 190 and 150 nm are found above regions 1R, 1G, and 1B.

FIG. 3 partially shows as an example and in the form of a circuit the conventional structure of a photodiode array intended for forming an image sensor. Each photodiode Dij is connected by its anode to the ground and by its cathode to the source of a precharge transistor Pij, the drain of which is connected to a reference voltage VR and the gate of which is connected to a row line Ri meant to select all the transistors Pij of a same row. Thus, in a first phase, diodes Dij are precharged. Then, after lighting, the voltage across the diodes is read by means of an amplifier formed, for example, of a first transistor Tij, the gate of which is connected to the connection node of transistor Pij and diode Dij, the source of which is connected to a column line Cj and the drain of which is connected to a high voltage Vdd. Each line Cj is connected to an amplifier Aj forming for example with transistor Tij a follower amplifier.

In such a structure, each diode Dij can be of the type described in connection with FIGS. 1A–1B, that is including a diode in parallel with a capacitor (not shown in FIG. 3).

An example of realization of a precharge transistor Pij and of a diode Dij is illustrated in FIG. 4. This structure is formed in a P-type single-crystal silicon substrate 10. Each transistor Pij includes an N-type drain region 11 and an N-type source region 12. Source region 12 extends to form the cathode region of diode Dij, the anode of which corresponds to substrate 10. Between the drain and the source of transistor Pij is formed an insulated gate 13, for example, made of polysilicon. The interference filter structure including layers 4, 5, and 6 already described in relation with FIG. 1 extends above most of region 12. Drain region 11 forms one piece with metallization 15 establishing a contact with a precharge voltage source VR.

Source/cathode region 12 forms one piece with a metallization 16 connected to the gate of transistor Tij (see FIG. 3). Further, and according to the present invention, polysilicon region 5 is connected to substrate 10. More currently, each of these regions will be connected to a common ground.

According to an alternative of the present invention, the diodes can be formed in a well itself formed in a substrate, that is, considering FIG. 4, P region 10 is a well formed in an N-type substrate not shown. In this case, polysilicon region 5 can be connected to the substrate and not directly to region 10.

Of course, the present invention is likely to have various alterations, modifications, and improvements which will readily occur to those skilled in the art. In particular, the various described materials may be replaced with equivalent materials. Other materials compatible with the manufacturing of semiconductor components may be used to make the interference filter formed above each diode. A significant feature of the present invention is that one layer of this interference filter, separated from the semiconductor substrate by an insulating layer, is conductive and is connected to the substrate. All the described types of conductivity may be inverted. Further, although a silicon substrate has been described, it should be noted that other semiconductor systems may be adapted to the implementation of the present invention.

Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the spirit and the scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The present invention is limited only as defined in the following claims and the equivalents thereto.

What is claimed is:

1. An array of photodiodes made of regions of a second conductivity type formed in a semiconductive region of a first conductivity type, divided into three interleaved sub-arrays, each sub-array corresponding to a respective color of light, all photodiodes of a respective sub-array being coated with a same interference filter including at least one insulating layer of determined thickness coated with at least one conductive layer, a combined thickness of the at least one insulating layer and the at least one conductive layer being different for each sub-array, the determined thickness of said at least one insulating layer and said at least one conductive layer coating the respective sub-array determining the respective color of light that is interferentially filtered and provided to the respective sub-array, wherein the determined thickness of said at least one insulating layer is proportional to a wavelength of the color of light that is interferentially filtered, wherein said at least one conductive layer is electrically connected to the semiconductive region of the first conductivity type.

2. The array of photodiodes of claim 1, wherein the electric connection is indirect.

3. The array of photodiodes of claim 1, wherein the semiconductor substrate is a single-crystal silicon substrate, and the interference filter includes a silicon oxide layer formed above the substrate and a conductive polysilicon layer formed above the silicon oxide layer.

4. The array of photodiodes of claim 1, wherein the semiconductive region of the first conductivity type comprises a semiconductor substrate made of single-crystal silicon.

5. The array of photodiodes of claim 1, wherein said at least one insulating layer comprises a silicon oxide layer.

6. The array of photodiodes of claim 1, wherein said at least one conductive layer comprises a polysilicon layer.

7. The array of photodiodes of claim 1, further comprising a silicon nitride layer over said at least one conductive layer.

8. The array of photodiodes of claim 1, wherein said semiconductive region of the first conductivity type comprises a semiconductor substrate made of single-crystal silicon, said at least one insulating layer comprises a silicon oxide layer, and said at least one conductive layer comprises a polysilicon layer.

9. The array of photodiodes of claim 8, further comprising a silicon nitride layer over said at least one conductive layer.

10. The array of photodiodes of claim 9, wherein said single-crystal silicon layer and said polysilicon layer have a

high refraction coefficient on the order of 4, while said silicon oxide layer and silicon nitride layer have a lower refraction coefficient, on the order of 1.5.

11. The array of photodiodes of claim **1**, wherein said at least one conductive layer is connected to said semiconductive region of the first conductivity type at a heavily doped P-type region thereof.

12. The array of photodiodes of claim **1**, wherein the at least one insulating layer includes a first insulating layer and a second insulating layer disposed below the first insulating layer, the first insulating layer extending across three photodiodes each in a different one of the three interleaved sub-arrays, and the second insulating layer extending across at least two photodiodes of the three photodiodes, wherein said at least on conductive layer extends across each of the three photodiodes above the first insulating layer.

13. The array of photodiodes of claim **12**, wherein the at least one insulating layer further includes a third insulating layer, disposed below the second insulating layer, that extends across only one of the three photodiodes.

14. The array of photodiodes of claim **1**, wherein said at least one insulating layer extends across three photodiodes each in a different one of the three interleaved sub-arrays, and wherein the determined thickness of said at least one insulating layer above each photodiode of the three photodiodes has a different thickness to interferentially filter a different wavelength of light.

15. The array of photodiodes of claim **1**, wherein each of the photodiodes of each respective sub-array has a capacitance, and wherein said at least one conductive layer of the interference filter coating the respective sub-array forms a capacitance in parallel to the capacitance of each of the photodiodes of the respective sub-array.

16. The array of photodiodes of claim **1**, wherein a thickness of said at least one conductive layer is substantially the same for each sub-array.

* * * * *